San Francisco State University
Electrical Engineering

Course Outline for Electronics (ENGR353)

Fall 2010

Bulletin Description:

Engr 353 Electronics
Prerequisite: grades of C or better in Engr 205 and 206. Concurrent enrollment in Engr 301. PN diodes, BJTs, and MOSFETs. Semiconductor device basics, characteristics, and models. Diode applications. Transistor biasing, basic amplifier configurations, and basic logic circuits.

PSpice simulation.

Textbook

Sergio Franco, Engr 353 Notes: **An Introduction to Microelectronics**, distributed by the University Reader

Reference

1. Behzad Razavi **Fundamentals of Microelectronics** Wiley, 2008 (ISBN:0471478466)
2. R. T. Howe and C. G. Sodini**, Microelectronics: an Integrated Approach,** Prentice-Hall, 1997.
3. Sergio Franco, **Electric Circuits Fundamentals**, Oxford University Press, 1995
4. Joseph G. Tront.: **PSPICE for Basic Microelectronics**, McGraw-Hill, 2008.
5. Sedra and Smith: **Microelectronic Circuits 3rd Ed**, Oxford University Press, 1989

Coordinator:

Hao Jiang, Assistant Professor of Electrical Engineering

Prerequisites by Topic:

1. Circuit analysis techniques (Ohm's law, KVL, KCL, and the superposition principle)
2. Ideal op amp circuits and the Op Amp Rule
3. Circuit equivalence and modeling concepts
4. Basic physics and electricity.
5. Familiarity with the basics of PSpice simulation

Course Objectives[1]:

1. To study *pn* junction diodes and basic applications thereof [A1, A.2, B.1, B.4]
2. To study transistors (BJTs and FETs), as well as their applications as single-stage amplifiers and logic inverters [A.1, A.2, B.1, B.4]
3. To expose students to SPICE simulation of basic op amp, diode, and transistor circuits [B.3]

[1]Indices in brackets refer to educational objectives and outcomes of the School of Engineering.

Topics:

1. Diodes: ideal diode characteristics and applications, physical operation of *pn* junctions, circuit analysis, dc and ac diode models, voltage references and dc power supply design. SPICE simulation
2. Bipolar junction transistors: physical operation, characteristics, models, biasing, single-stage amplifier configurations, switch and logic applications, SPICE simulation.
3. Field-effect transistors: physical operation, characteristics, models, biasing, single-stage amplifier configurations, CMOS inverters and switches, SPICE simulation

Professional Component:

1. Engineering Sciences: 67%
2. Engineering Design: 33%

Performance Criteria:

Objective 1
1.1 Students will become conversant with *pn* junction behavior and characteristics. [1, 2]
1.2 Students will demonstrate an ability to analyze diode circuits using graphical and iterative techniques as well as large-signal and small-signal models. [1, 2]
1.3 Students will demonstrate a knowledge of popular diode applications such as rectification, regulation, limiting, and clamping. [1, 2]
1.4 Students will become conversant with SPICE diode models. [1]
Objective 2
2.1 Students will become conversant with the physical structures of BJTs, and MOSFETs, as well as their electrical characteristics. [1, 2]
2.2 Students will demonstrate an ability to use large-signal models for the DC analysis and design of simple transistor circuits. [1, 2, 3]
2.3 Students will demonstrate an ability to use small-signal models for the analysis and design of basic single-stage amplifiers. [1, 2, 3]
2.4 Students will demonstrate an ability to analyze simple logic inverters using transistors. [1, 2, 3]
2.5 Students will become conversant with SPICE transistor models. [1]
Objective 3
3.1 Students will demonstrate a skill in running successful computer simulations of simple electronic circuits and compare with hand calculations. [1]

Instructor: Hao Jiang, Ph.D.

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Notes on Prerequisites

Engineering students must have a copy of the course approval form on file. Non-engineering students must submit a copy of the grade report showing the appropriate course grade for ENGR 205 and 206.

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Relationship to Other Courses

This course extends the introductory circuit coverage of Engr 205 to electronic devices (diodes and transistors.) It prepares the student for Engr 301, 445, 453, and 455. Most of the Engr 353 material is put to use in the Engr 301 lab, which is taken concurrently with (or after) Engr 353.

Important note

If you are taking Engr 353 and Engr 301 concurrently, and decide to withdraw ***from Engr 353, you will automatically be dropped also from Engr 301.***

Disability Statement Policy

Students with disabilities who need reasonable accommodations are encouraged to contact the instructor. The Disability Programs and Resource Center (DPRC) is available to facilitate the reasonable accommodations process. The DPRC is located in the Student Service Building and can be reached by telephone (voice/TTY 415-338-2472) or by email (dprc@sfsu.edu). For more information, please check http://www.sfsu.edu/~dprc.

Observance of Religious Holidays

I will make reasonable accommodations for students to observe religious holidays when such observances require students to be absent from class activities. Please inform your absence ahead of the time so that I can make some arrangements.

Rules

1. No make-up exams will be given without valid unavoidable reason with valid documented proof from a doctor, police officer, Court, etc.
2. If any student is **caught cheating as specified by the university handbook**, I will **report it to the department and strongly recommend University policy** including a **final grade of "F"** in the course.

The Laboratory and Projects rules will be handed out in the laboratory section

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Proposed Schedule

Table 1: A tentative schedule about instruction topics, quiz and homework

Week	Topics	Quiz	HW
1.5	Introduction		
2.1	The basic diode application		
2.3	More diode applications		
3.3	Semiconductors and semiconductor resistors		1
4.1	Diffusion, space charge layer, diode equations	1	
4.3	DC analysis of the diode		2
5.1	Voltage regulation and DC power supply	2	
5.3	BJT device structure		3
6.1	Mid Term 1 (9/27)		
6.3	Mid Term 1 Review		
7.1	i-v of BJTs Operating regions and BJT models	3	
7.3	BJT circuits		4
8.1	BJT as an amplifier/switch	4	
8.3	small signal of BJTs		5
9.1	The BJT as a resistance-transformation device	5	
9.2	BJT Biasing for amplifier design		6
10.1	Basic BJT amplifiers with CE configuration	6	
10.3	CE with emitter-degeneration		7
11.1	Mid Term 2 (11/1)		
11.3	Mid Term 2 Review		
12.1	Common Collector BJT circuits	7	
12.3	Common Base BJT circuits		8

Week	Topics	Quiz	HW
13.1	MOSFET structure, VTH and p-MOSFET models	8	
13.3	MOSFET in resistive DC circuits		9
	Break		
14.1	small signal operation of MOSFETs	9	
14.3	Basic MOSFET amplifiers with diode load		10
15.1	Basic MOSFET amplifiers with current source		
15.3	Common drain MOSFET amplifiers		
16.1	Common base MOSFET amplifiers	10	

Evaluation:

Exam	Date	Time	Total of Grade
Mid Term 1	9/27	14:10-15:25	20%
Mid Term 2	11/1	14:10-15:25	20%
Final	12/12 week	2.5 hour	30%

1. No late homework accepted. Solutions to the homework assignments are posted in the solution window across Sci 144.
2. All exams are closed book. *No electronic devices* (cellular phones, PDAs, iPODs, etc.) allowed, except for a basic calculator.
3. ***No make-up exams*** and ***no incomplete grades*** without a *serious and verifiable medical justification*..

Table 2: The grade criteria

Item	Points	Comments
Homework	10	Each homework assignment has 3 problems Each homework assignment is 1 point; Turn in homework in class on time has 0.5 point; No late homework will be accepted.
Quiz	20	Quiz on Wed. (10 min) has 1 problem (10-15min); Attendance counts 1 point;
Mid Term 1	20	75 min. 4 problems

Item	Points	Comments
Mid Term 2	20	75 min. 4 problems
Final	30	2 hours

Table 3: The letter grade is based on the following table.

A	A-	B+	B	B-
>90%	85% ~ 89%	80% ~ 84%	75% ~ 79%	70% ~ 74%

C+	C	C-	D+	D	D-
65%~69%	60%~64%	55%~59%	50%~54%	45%~49%	40%~45%