San Francisco State University
Electrical Engineering

Course Outline for Design with Operational Amplifiers (ENGR442)

Spring 2014

Bulletin Description:

442 Design with Operational Amplifiers (3) Spring
Prerequisite: grades of C or better in Engr 205, concurrent enrollment in Engr 305. Design of op-amp based amplifiers, signal converters, conditioners and filters. Negative feedback, practical op-amp limitations. Voltage comparators, Schmitt triggers, nonlinear signal processing. Sinewave oscillators, multivibrators, function generators. Design project involving PSpice **s**imulation.

Prerequisites:

Engineering students must have a copy of the course approval form on file ("C-" or better in ENGR305).

Prerequisites by Topic:

1. Circuit analysis techniques with dependent sources, equivalence
2. Basic systems analysis concepts using Laplace techniques and Bode Plots
3. Transient and frequency response of 1st-order circuits
4. Ability to use PSpice for simple circuit simulations

Textbook

Sergio Franco, Design with Operational Amplifiers and Analog ICs, 3rd Ed., WCB/McGraw-Hill, 2002

Coordinator:

Hao Jiang

Instructor: Hao Jiang,

Office: TBD; Office Hrs: Wed: 2:00-5:00 pm, or by appointment
Phone: (415)338-6379; E-mail: jianghao@sfsu.edu;

Course Objectives[1]:

1. To investigate a variety of resistive op amp circuits with emphasis on feedback principles. [A,1, B.1, B.4]
2. To analyze and design active filters [A.1, B.1, B.4]
3. To investigate the effect of op amp nonidealities upon the DC as well as the AC and transient responses of popular op amp circuits [B.1]

4. To study the design of popular op amp and comparator applications in test, control, and instrumentation [B.1]
5. To perform SPICE simulation of common analog circuits [B.3]
[1]Indices in brackets refer to educational objectives and outcomes of the School of Engineering.

Topics:

1. Review; basic closed-loop configurations; negative feedback; op amp powering and saturation.
2. *I-V*, *V-I*, and *I-I* converters; difference and instrumentation amplifiers.
3. 1st-order filters. 2nd-order active filters: *KRC*, multiple feedback, state-variable and biquads.
4. Input-referred DC errors, drift, CMRR and PSRR; operating limits.
5. Frequency response, input /output impedances, small- and large-signal transient responses.
6. Voltage comparators and Schmitt triggers; precision rectifiers.

Professional Component:

1. Engineering Sciences: 67%
2. Engineering Design: 33%

Performance Criteria:

Objective 1
1.1 Students will become conversant with *pn* junction behavior and characteristics. [1, 2]
1.2 Students will demonstrate an ability to analyze diode circuits using graphical and iterative techniques as well as large-signal and small-signal models. [1, 2]
1.3 Students will demonstrate a knowledge of popular diode applications such as rectification, regulation, limiting, and clamping. [1, 2]
1.4 Students will become conversant with SPICE diode models. [1]
Objective 2
2.1 Students will become conversant with the physical structures of BJTs, and MOSFETs, as well as their electrical characteristics. [1, 2]
2.2 Students will demonstrate an ability to use large-signal models for the DC analysis and design of simple transistor circuits. [1, 2, 3]
2.3 Students will demonstrate an ability to use small-signal models for the analysis and design of basic single-stage amplifiers. [1, 2, 3]
2.4 Students will demonstrate an ability to analyze simple logic inverters using transistors. [1, 2, 3]
2.5 Students will become conversant with SPICE transistor models. [1]
Objective 3
3.1 Students will demonstrate a skill in running successful computer simulations of simple electronic circuits and compare with hand calculations. [1]

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Evaluation:

Item	Points	Comments
Attendance	6	Random attendance checking
Homework	8	Each homework assignment is 1 points; No late homework will be accepted;
Review	16	Each Review is 2 points Attendance counts 1 point; Performance counts 1 points
Mid Term 1	15	50 min
Mid Term 2	15	50 min
Mid Term 3	15	50
Final	25	2.5 hours

Rules:

1. No late homework will be accepted.
2. There are about 8 review session, but the total score of the quiz will be capped as 20%
3. **If you miss 3 attendance (counted by homework and quiz) consecutively, YOU WILL BE DROPPED**.
4. The final result in the exam must be written in ink-pen with a circle or a box.
5. All exams are closed book. No electronic devices (cellular phones, iPAD, etc.) allowed, except for a basic calculator.
6. No make-up exams and no incomplete grades without a serious and verifiable medical justification

Exam	Date	Time	Total of Grade
Mid Term 1	TBD	11:10-12:00	15%
Mid Term 2	TBD	11:10-12:00	15%
Mid Term 3	TBD	11:10-12:00	15%
Final	5/19(Mon)	10:45-13:15	25%

Table 3: The letter grade is based on the following table.

A	A-	B+	B	B-
>90%	85% ~ 89%	80% ~ 84%	75% ~ 79%	70% ~ 74%

C+	C	C-	D+	D	D-
65%~69%	60%~64%	55%~59%	50%~54%	45%~49%	40%~45%

Relationship to Other Courses

Engr 442 is a required course of all EE majors. It complements the analog design viewpoint of Engr 445. While Engr 445 focuses on device design aspects of analog ICs, Engr 442 concentrates on systems design aspects and applications. Together, these courses are designed to provide the student with a fairly comprehensive undergraduate background in analog electronics with emphasis on design.

Disability Statement Policy

Students with disabilities who need reasonable accommodations are encouraged to contact the instructor. The Disability Programs and Resource Center (DPRC) is available to facilitate the reasonable accommodations process. The DPRC is located in the Student Service Building and can be reached by telephone (voice/TTY 415-338-2472) or by email (dprc@sfsu.edu). For more information, please check http://www.sfsu.edu/~dprc.

Observance of Religious Holidays

I will make reasonable accommodations for students to observe religious holidays when such observances require students to be absent from class activities. Please inform your absence ahead of the time so that I can make some arrangements.