San Francisco State University
Electrical Engineering

Course Outline for Electronics (ENGR445)

Fall 2014

Bulletin Description:

445 Analog Integrated Circuit Design (4) F
Prerequisite: grades of C or better in ENGR 301 and 353. Integrated circuit technology, transistor characteristics and models. Analysis and design of monolithic op amps. Frequency response, negative feedback, stability, PSpice simulation. Classwork, 3 units; laboratory, 1 unit. Extra fee required.

Textbook

Tony Chan Carusone, David A. Johns, and Kenneth W. Martin, **Analog Integrated Circuit Design 2nd Edition** *(It is important to get the 2nd edition)*. Wiley, 2011 (ISBN: 0470-77010-4)

Reference

1. Philip Allen and Douglas Holberg, **CMOS Analog Circuit Design 3rd**, Oxford Press, 2011
2. Behzad Razavi **Design of Analog CMOS Integrated Circuits** McGraw-Hill, 2000

Coordinator:

Hao Jiang, Associate Professor of Electrical Engineering

Prerequisites by Topic:

1. Basic semiconductor theory, *pn* junction, MOSFET, and BJT fundamentals
2. Circuit analysis techniques with dependent sources, concept of equivalence
3. Basic systems theory, frequency and time responses, Bode Plots
4. Ability to use PSpice for simple transistor circuit simulations

Professional Component:

1. Engineering Sciences: 50%
2. Engineering Design: 50%

Instructor: Hao Jiang, Ph.D.

Office: SCI 213C; Office Hrs: MWF 10-11am, or by appointment
Phone: (415)338-6379; E-mail: jianghao@sfsu.edu;

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Proposed Schedule

No	Topics	Notes
1	MOSFET: Voltage controlled current source	
2	MOSFET: Saturation	
3	MOSFET: PMOS	
4	MOSFET: Body Effect	
5	MOSFET: Model Card	
6	Review #1	Lab starts
7	Basic Blocks: Current Source	
8	Basic Blocks: Common Source Amplifier	
9	Basic Blocks: Common Drain Amplifier	
10	Basic Blocks: Common Gate Amplifier	
11	Review #2	
12	Cascode Current Source	
13	Casecode Amplifier Gain	
14	Review #3	
15	Differential Pair	
16	Review #4	Midterm 1
17	MOSFET: Capacitance	
18	Bode Plot	
19	Frequency Response: Common Source	
20	Frequency Response: Common Gate	
21	Review #5	
22	Frequency Response: Cascode	
23	Frequency Response: Differential Pair	

No	Topics	Notes
24	Frequency Response: Common Drain	
25	Review #6	Midterm 2
26	Feedback: Generic Negative Feedback System	
27	Feedback: Frequency Response and Phase of an Amplifier	
28	Review #7	
29	Basic Operational Amplifier Design	
30	Compensation	
31	Review #8: A design procedure	
32	Wide Swing Current Source	
33	Wide Swing Amplifier Design	
34	Bandgap Circuit	

Evaluation:

1. 10 homework assignments; 10% of lecture grade
2. 10 quizs; 20% of lecture grade
3. 2 mid terms; 40% of lecture grade
4. 1 final (Dec. 18th, 8:00~10:30 am) ; 30% of lecture grade
5. Overall grade = 75% of lecture grade + 25% of lab grade

Notes on Evaluation

1. No late homework accepted.
2. All exams are closed book. *No electronic devices* (cellular phones, PDAs, iPADs, etc.) allowed, except for a basic calculator.
3. ***No make-up exams*** and ***no incomplete grades*** without a *serious and verifiable medical justification*.
4. **You will be dropped if you miss 3 classes in a roll without permission.**

Table 2: The letter grade is based on the following table.

A	A-	B+	B	B-
>90%	85% ~ 89%	80% ~ 84%	75% ~ 79%	70% ~ 74%

C+	C	C-	D+	D	D-
65%~69%	60%~64%	55%~59%	50%~54%	45%~49%	40%~45%

Notes on Prerequisites

Engineering students must have a copy of the course approval form on file. Non-engineering students must submit a copy of the grade report showing the appropriate course grade for ENGR 353 and 301.

Relationship to Other Courses

This course extends ENGR 353 and complements ENGR 442. While ENGR 442 focuses on analog systems design, ENGR 445 concentrates on device design aspects. This correspondence in the analog realm mirrors the correspondence between ENGR 453 and ENGR 478 in the digital realm. Together, these courses provide students with a fairly comprehensive background in microelectronics with emphasis on design.

Disability Statement Policy

Students with disabilities who need reasonable accommodations are encouraged to contact the instructor. The Disability Programs and Resource Center (DPRC) is available to facilitate the reasonable accommodations process. The DPRC is located in the Student Service Building and can be reached by telephone (voice/TTY 415-338-2472) or by email (dprc@sfsu.edu). For more information, please check http://www.sfsu.edu/~dprc.

Observance of Religious Holidays

I will make reasonable accommodations for students to observe religious holidays when such observances require students to be absent from class activities. Please inform your absence ahead of the time so that I can make some arrangements.